In the "Response to Applicants' Remarks", the Examiner notes that Doyle teaches that it is not a requirement that the source/drain regions be silicided (Col. 3, lines 55-64). Applicants note that Doyle neither states, nor implies that it is not a requirement that the gate region be silicided. The Examiner asserts that since it is not a requirement that the source/drain regions be silicided, then the silicide layer 110, is not needed. Applicants respectfully submit that the silicide layer 110 goes to the heart of the Doyle patent, and without it, there is no need for the patent.

At the outset, in the "Description of the Invention", Doyle states that "The present invention relates generally to microelectronic structures and fabrication methods, and more particularly to the formation of a *low resistance gate electrode* layer (emphasis added). Having disclosed the purpose of the invention, the Applicants' ask the Examiner to consider whether a low resistance gate electrode can be formed (according to Doyle) without the formation of a silicide on the gate electrode.

In the "Background of the Invention", Doyle presents shortcomings associated with gate electrodes of polysilicon, and concludes the section by stating "What is needed is a structure that provides low resistance gate electrodes, and methods of making such a structure" (Col.1, lines 55-57). The answer is stated briefly in the first paragraph in the section entitled "Summary of the Invention". Particularly, and unequivocally, Doyle states "Briefly, a

MOSFET having a low resistance gate electrode structure includes a silicided gate electrode" (Col.1, lines 59-64).

Based on the above, Applicants submit that it is clearly established that a silicide layer in the gate electrode is an absolute requirement of the Doyle patent. Having thus established this fact, Applicants address the issue of whether silicide layer 110 is required, even though silicided source/drain regions are not required.

Toward this end, the Abstract of Doyle states that a MOSFET having a low resistance gate electrode structure includes a silicided gate electrode wherein the *thickness of the silicide layer superjacent the gate electrode* is *substantially thicker* than the silicide layers overlying the source and drain regions (Col.2, lines 1-3). Further, Doyle states that a nickel layer 116 is reacted with the underlying polysilicon to form a new silicide layer 118 that is *substantially thicker than silicide layer 110* (Col.3, lines 24-28). In another portion Doyle discloses that a MOSFET having a low resistance gate electrode structure includes a silicided gate electrode wherein the *thickness of the silicide layer superjacent a polysilicon gate electrode* layer is *substantial in comparison to the polysilicon* (Col.1, lines 59-64).

It is obvious then, that the desired thickness of the silicide layer 118 is achieved by the double silicide process as opposed to a single silicide process. It has already been observed that a single silicide process produces a thin silicide layer such as gate silicide 110 and source/drain silicides 112.

Therefore, Applicants respectfully submit that the correct conclusion, supported by the Doyle patent, is that while source/drain silicides 112 are not required, gate silicide 110 is essential to form a silicide of the desired thickness. Those skill in the arts will recognize that there are numerous ways to form gate silicide 110 without forming source/drain silicides 112. A further conclusion (a quite obvious conclusion) is that source/drain silicides 112 do not contribute to, and therefore are not required for the formation of a silicided gate electrode wherein the thickness of the silicide layer superjacent a polysilicon gate electrode layer is substantial in comparison to the polysilicon.

Therefore, Applicants respectfully reassert that Doyle fails to teach forming a first silicide pattern on the non-silicide gate without etching a silicide from which the silicide pattern is fabricated, as recited in independent claim 21, as amended. Reconsideration and withdrawal of this art grounds of rejection are respectfully requested.

Rejections under 35 U.S.C. § 103

Claims 1-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Doyle in view of Broadbent et al. (IEEE Transactions on Electron Devices Vol. 36.No.11, November 1989). This rejection is respectfully traversed.

Based on the arguments set forth above with respect to the rejection under 35 U.S.C. 102, it is clear that the silicide layer 110 is essential to the Doyle

patent, and that the sacrificial dielectric layer 114 is formed on the silicide layer 110, which isolates it from contact with the surface of the polysilicon portion of the gate electrode. Therefore, Applicants respectfully reasserts that Doyle does not teach or suggest forming an insulating film thicker than the gate on said exposed top and side surfaces and on an entire surface of the substrate, as recited in independent claim 1, as amended, and similarly stated in independent claim 10 (as amended). Broadbent et al. cannot fill this vacancy.

Claims 2-9 and 11-20 depend, either directly or indirectly on independent claims 1 and 10. Since neither Doyle, nor Broadbent et al. discloses or suggest forming an insulating film thicker than the gate on said exposed top and side surfaces and on an entire surface of the substrate, Doyle in view of Broadbent et al. cannot render claims 1-20 obvious to one of ordinary skill in the art. Reconsideration and withdrawal of this art grounds of rejection are respectfully requested.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone Percy L. Square, Registration No. 51,084, at (703) 205-8034, in the Washington, D.C. area.

Prompt and favorable consideration of this Amendment is respectfully requested.

Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), the Applicants respectfully petition for a one (1) month extension of time for filing a response in connection with the present application and the required fee of $110.00 is attached herewith.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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